Status of Upgraded Pixel Test System

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Wafer probing rad-hard chips requires new test system:

- Need ability to test chips at elevated clock speeds to simulate post-rad performance.
- Need ability to measure margins on timing and amplitude of all input and output signals using “IC tester” approach with a special PCC (PICT = Pixel IC Tester)

Production module testing also requires new test system:

- Very efficient module testing during production.
- Connection to production modules with no support card.
- Full monitoring of relevant quanitites (current reference, current and voltage mode DAC outputs, and temperature monitoring)
- Need PCC to support production burn-in as well (highly multiplexed system).

Test System Upgrades

Two major goals:

- Design evaluation and production probing of rad-hard chips: Determining that a given die has high probability to meet specifications after irradiation requires initial testing be done parametrically, to see if performance margin is adequate.
- Production testing requires some new issues to be addressed. These include interconnect issues and burn-in issues, among others.

Discuss proposal in terms of three boards:

- Upgraded PLL (TurboPLL): A new version needs to be produced for IC testing. Several issues need to be addressed, including: larger SRAM for module testing, more programming capability, higher speed operation of devices under test. Goal for operating speed would be up to 100MHz XCK.
- Upgraded PCC (TurboPCC): A new version will be needed for production testing. Some issues that would need to be addressed include: higher speed operation of devices under test, and multiplexed operation of many modules for burn-in.
- Pixel IC Tester (PICT): This new “PCC-like” board is needed to allow complete parametric characterization of FE chips and modules. Some of the parameters to be varied include operating frequency (XCK), voltage margins for I/O, and timing/phasing margins for I/O.

More detailed list of proposed upgrades:

TurboPLL:

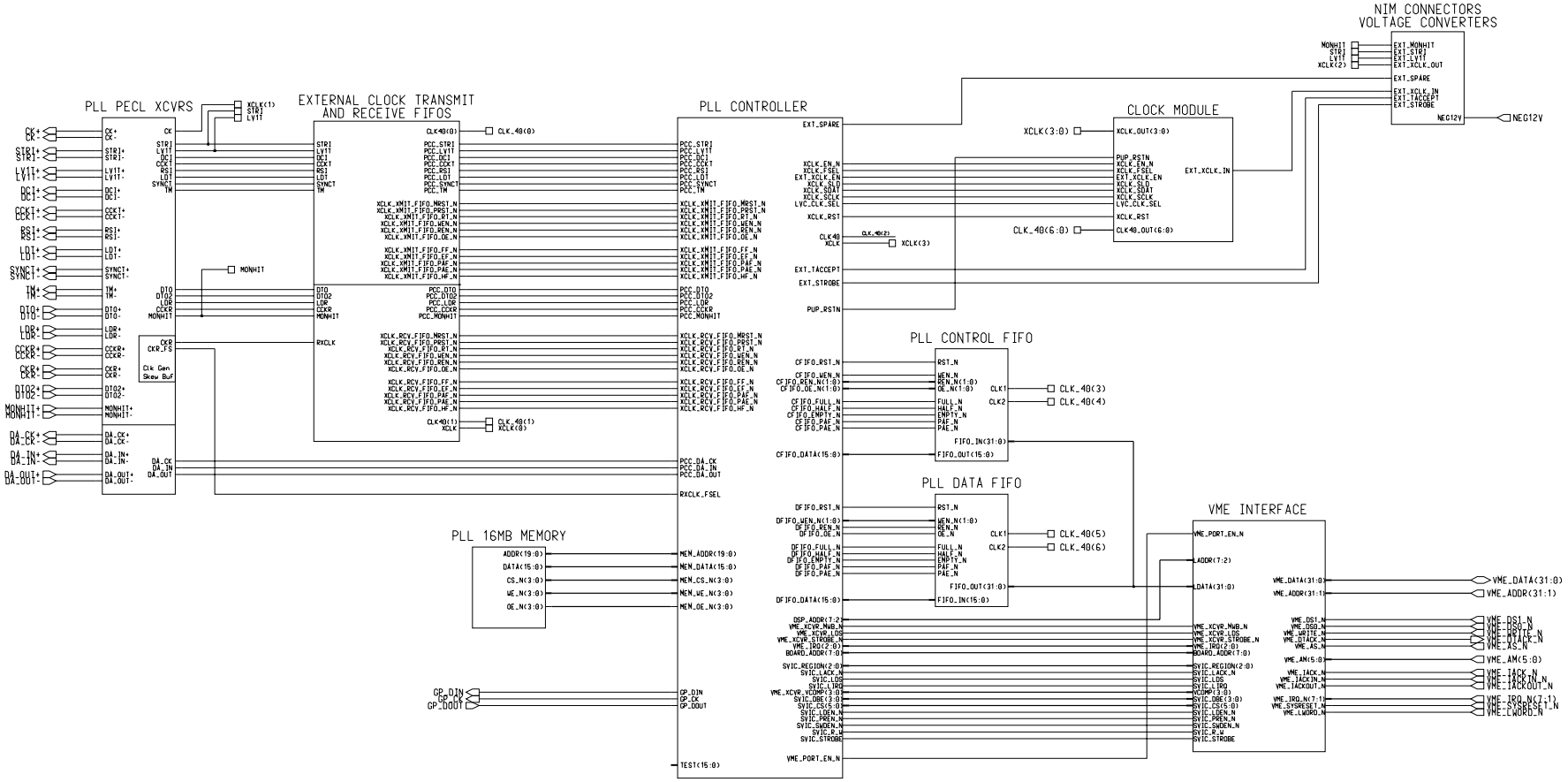
- Replace the current ORCA2C40 FPGA with a Xilinx Virtex part XCV300. This gives significant increase in available gates as well as significant increase in speed, plus very useful RAMblocks. This is a 2.5/3.3V BGA part.
- Remove the old DSP interface to free board space and front-panel space
- Add two large FIFOs between cable drivers/receivers and the PLL core. This allows operation of device under test at elevated XCK frequency without operating the PLL itself at the same high frequency. The output is XFIFO, the input is RFIFO. The new IDT SuperSync II parts (512Kx9 bit, 133MHz) are ideal.
- Add programmable clock generation for outgoing XCK using Synergy SY89429 part with large frequency range. Also add improved clock recovery from XCKR using Cypress CY7B9911V PLL. The clock range should be 7.5MHz - 110MHz.
- Add more NIM outputs to provide XCK, STROBE, and LV1 outputs.
- Upgrade internal histogramming SRAM to support module level histogramming. This requires going from 2MB to 16MB SRAM on board, plus using a simple address mapping. This will be done with 8 of the new Toshiba 16Mbit SRAM (TC55V8200-12). Lab tests indicate that this extra RAM would increase module threshold scan speed by almost a factor of three.
- Provide support for DTO2, the second data stream from the production MCC.

- Provide support for HitBus as a true data signal. This would allow the PLL to do Hitbus-based threshold scans of an FE chip with XCK on/off (XCK would still propogate to the PCC, and then return, to keep operation of PLL straighforward). A simple algorthm, such as used by Bonn, is to count HitBus rising edges within a window after STR rising edges.

Comments on X/R FIFOs between cable and FPGA:

- This provides greatly improved flexibility, but also is complex to operate when the clock frequencies on the FPGA and FIFO are different.
- One mode of operation is to lock the FPGA and FIFO clock together, and then the board can be operated much like the present PLL.
- When the frequencies are different, we imagine effectively translating individual primitives from the CFIFO into waveforms in the XFIFO, and then bursting them out. Presently, we don't plan to overlap the loading and transmission from XFIFO.
- For a typical trigger sequence (INT_DATA or EXT_DATA command), the waveforms can be very long (100 triggers with 200μs interval is 20ms), and largely composed of delays. Here, we propose to load the waveform for one event, and use the ReTransmit feature on the FIFO to send it at regular intervals. Extra pauses would be automatically generated by the FPGA to keep the RFIFO from overflowing, since the FPGA can no longer keep up with the incoming data stream if its clock is running at a lower frequency.

Overview of major blocks in new PLL:



TurboPCC:

- Replace ORCA FPGA with small Xilinx XCV100 part.
- Provide support for device under test without XCK (special HitBus testing)
- Provide improved strobe delay support using two AD9501 programmable delay generators to control edge delays, and digital pots to control the total delay from the PLL. This would give more flexibility in timewalk scanning.
- Provide improved DAC support by using a 14-bit DAC (MAX5170 + MAX6325) to give 0.25mV step size over a 4V range. Also use two DACs to separately control VHigh and VLow for chopper. Presently, use a resistive divider to divide the PCC output by 5 on the single-chip and module support cards to provide smaller steps for threshold scans, but then the maximum charge is very limited. This improved dynamic range would eliminate the need for dividers.
- Provide on-board chopping using the AD8180 and AD8009 video chopper and high speed buffer. These devices have better chopping performance (faster, and better dynamic range) than the MAX4313 we now use as an “add-on” board.
- Provide support for second DTO2 line to support production MCC. Note at the moment, the 50-pin R/N connector used on all support cards has no room for this connection, without loss of backwards compatibility...
- Provide support for final testing connection to modules (perhaps this is a special pigtail with R/N connector on one end and Elco5087 test connector on the other).

- Production test connection proposal is to use a “mini-support card” with the standard 50-pin Robinson-Nugent connector, a VCal LEMO and an HV LEMO, which are connected to the Elco5087 test connector on the Flex 2.x .
- Production modules will have a single pair of temperature measurement lines. Appropriate circuitry should be provided to digitize temperature (sensor expected to be a 10K 1% precision NTC thermistor). This is best done with a standard sigma/delta ADC such as the AD7711. The ADC includes digital filtering and self-calibration and provides a voltage reference. Two additional resistors are used to limit self-heating and linearize the response over the relevant temperature range.

For production, will want an extended PCC for burn-in tests:

- Provide support for multiplexed burn-in testing. Support connection to 16 modules. All modules would receive XCK and DCI. One module at a time could multiplex DTO back to PLL for complete testing. This would allow cycling continuously through group of modules to monitor in real time if any fail.
- Would need to include a system for power supply voltage and current monitoring of individual modules (similar to what is proposed for PICT - see later).
- Assume that it would be acceptable to operate such a card off of single large bulk supplies for the VDD/VDDA/VCCA (15-20A for each of these lines !). It seems unlikely that there will be production CAEN mainframes and supplies in all of the module test institutes, so support of some equivalent functions is needed in PCC.

Pixel IC Tester (PICT):

- Need to provide adequate capability for 100MHz operation. To properly synchronize signals before transmission to PLL, propose to add resync circuitry on the PICT board, so that signals are transmitted back to PLL with fixed timing relationship, independent of parameter settings on PICT.
- Propose to build individual “pin driver” circuits for testing FE I/O pads parametrically. The basic building blocks would include the AD53020 programmable delay control that allows adjustment of delay and width independently, and the AD53500 pin driver with adjustable high and low drive levels, and the AD53042 window comparator with adjustable high and low thresholds. These would be controlled by two AD5532 32-channel DACs.
- With these ingredients, the arrival time, width and amplitude could be varied for each of the input signals and measured for each one of the output signals.
- Imagine that standard tests would include register tests and digital hit injection (where output bit pattern is fully deterministic), with loops over operating parameters inside each test sequence. With proper design of the PLL-PICT slow control communication so that parameters can be quickly set, a sequence of such tests could be quite rapid. A binary search could be made to determine the maximum operating frequency for various tests.
- Need to investigate high-quality probe card designs for operation of devices under test at speeds up to 100 MHz. Passive needle-based cards seem OK.

Signals to be handled parametrically are:

- CMOS inputs (CCK, DI, LD, RSTb) with programmable delay, width and amplitude. Delay is programmable over about 30ns range, width can be separately changed by about 10ns, and low/high amplitude would be arbitrary.
- CMOS GA pins with programmable tristate CMOS drivers (check whether no connection gives high and ground connection gives low for GA bit).
- LVDS inputs (STR, XCK, LV1, SYNC) with programmable delay, width, and amplitude. Both sides of the differential pair would be controlled fully to allow simulating common mode offsets, relative timing shifts between two inputs, as well as amplitude changes.
- LVDS outputs (DO) with window comparator and programmable delay. Only DO needs to be fully evaluated. A fast differential amplifier would be used before the delay and comparator chips, to more accurately model an LVDS receiver.
- The implementation would take approximately 3 delay chips, 1 comparator chip, 12 pin driver chips, and 2 DAC chips, plus a moderate amount of level translation. This should fit on a modest size card near the device under test, but would have to be carefully engineered for 100MHz operation.

Configuration:

- Optimal configuration of cables and probe card design need study. Assume that a passive, well-designed probe card plus a short (20cm) cable to PICT will work. However, placing receiver circuitry on probe adapter card (opamps for monitoring and fast diffamp for DO output) may be needed to assure proper operation.

Monitoring capability:

- Need ability to monitor voltages and currents rapidly during testing. Propose to implement 16 channels of ADC monitoring.
- A relatively fast ADC with decent dynamic range will be used to allow rapid characterization of the DACs in the FE chips. The proposed solution uses the AD7856 8-channel, 14-bit DAC, which digitizes in 4-6μs. This chip includes extensive self-calibration capability. Would use low-offset opamps (AD8574) to provide low-impedance signal sources, and match into ADC dynamic range.
- Two ADC chips and 4 opamp chips, plus the necessary passive components would provide all of the needed functions.
- There are twelve analog pins on the FE chips to be analyzed during wafer probing. These include VCal, VCCD, VTH, MonRef, and I1-I8. Note that MonRef and I1-I8 are actually current sources, whereas the others are voltage sources.
- The remaining 4 channels of monitoring capability would be used to measure the currents on VDD, VDDA, VCCA, plus one additional quantity.

Status:

- Schematics completed for new PLL. Parts orders and board layout are underway. Hope to have the first prototypes working in the lab by early Sept. For the first round, we are ordering parts for 10 boards, and will initially fabricate a smaller number (about 3) to get them fully debugged.
- PICT is next card to do. It is presently a fairly detailed conceptual design. Work on schematics will start in 2-3 weeks. Hope to be ready to order parts and start board layout by end of July. Many circuits are in common with the new PCC (the new PCC is essentially a simplified subset of the PICT), so the schematics for both the PCC and the PICT can be done essentially in parallel.
- Present team is a full-time junior engineer and about 25% of a senior engineer, plus an engineering intern (undergraduate) to help on VHDL. Necessary financial support exists for construction of boards. J. Richardson and myself follow work in detail with frequent discussions and meetings.
- Goal would be to have first operational system by beginning of October for FE-D2 evaluation. This is an aggressive schedule, but essential if we want to fully evaluate the FE-D and FE-H chips and make sure they meet requirements.
- Significant amount of host (PixelDAQ) software upgrades also required.
- Not yet clear whether this should replace all present PLL systems or whether it will be built only in smaller quantities for wafer probing and specialized testing.